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10/783,347	02/20/2004	Hideyoshi Yoshimura	60836 (70904)	7701

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,347	YOSHIMURA, HIDEYOSHI	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/2/0/04 and 7/18/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/18/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 7-11, and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Dave et al. (hereinafter Dave) (US 6,112,023).

3. As to claim 1, Dave teaches an asymmetrical multiprocessor system comprising a plurality of processors for executing a plurality of unit jobs, workloads for which are foreseeable, the unit jobs being allocated job by job to the plurality of processors, at least a first processor and a second processor being asymmetrical to each other (see Abstract), the asymmetrical multiprocessor system comprising:

unit job processing information generating means for generating unit job processing information, which is used as reference information when the unit jobs are allocated to the plurality of processors (performance estimation information, such as relating to power, that is used to determine the allocation of jobs/tasks to the processing elements) (col. 2, lines 51-67, col. 3, lines 32-51, col. 4, lines 1-22); and

unit job scheduling means for determining, in accordance with the unit job processing information, in what order the unit jobs are to be executed, and to which processor the unit jobs

are to be allocated (scheduler based on priority in view of performance information is used for allocation) (col. 4, lines 1-37, col. 2, lines 51-67).

4. As to claim 2, Dave teaches wherein: at least one of the unit jobs is executable for the first processor and the second processor in accordance with programs that are different from each other (have heterogeneous platforms/architecture that have different costs) (col. 1, lines 35-45, Abstract).

5. As to claim 3, Dave teaches wherein: the unit job processing information includes information about power consumption of each of the processors; and in accordance with the information about power consumption, the unit job scheduling means determines to which processor the unit jobs are to be allocated, determination being done in such a manner that the power consumption is reduced (col. 3, lines 16-17, last three lines of the Abstract).

6. As to claim 7, Dave teaches wherein: the unit job processing information includes (i) information, with respect to each unit job, about an estimated value of time required for processing the unit job (performance estimation step estimates the finish time of each task) (col. 2, lines 59-67), (ii) information about dependency relations between the unit jobs (the job executed next is known by the scheduler, which has the execution order established by priority)

(Abstract, col. 2, lines 51-67, col. 5, lines 4-7), and (iii) information, with respect to each unit job, about which processor is capable of executing the unit job.

7. As to claim 8, Dave teaches wherein: the unit job scheduling means determines, at least at an end of each unit job, in what order the unit jobs are to be executed (scheduler basis scheduling on priority) (see Abstract, col. 2, lines 57-67, col. 3, lines 66-67 through col. 4, lines 1-3 and 29-38).

8. As to claim 9, Dave teaches wherein: the unit job scheduling means performs (i) a process of extracting the unit job (extracts/selects tasks from task graph) executable for one or more of the plurality of processors (allocates to one of the other processing elements) (col. 2, lines 51-67, col. 3, lines 32-51, col. 4, lines 1-22), (ii) a process of extracting the processor that is not yet scheduled which unit job to execute (col. 1, line 59), and (iii) a process of allocating, to the processor extracted, the unit job executable for the processor extracted (Abstract, col. 3, lines 66-67, col. 4, lines 1-37, col. 6, lines 38-39).

9. As to claim 10, Dave teaches the asymmetrical multiprocessor system as set forth in one of claims 1 and 2, wherein: the unit job scheduling means allocates a unit job to the second processor (Abstract, col. 2, lines 51-61), which is *capable of* executing at least the unit job, preferentially over the first processor, which is *capable of* executing more kinds of unit jobs than

the second processor is. It is noted that the above underlined intended use recitations do not receive any patentable weight (see MPEP 2106). Dave's job scheduler has the "capability" to perform the above intended use recitations.

10. As to claim 11, Dave teaches wherein: the unit job scheduling means allocates a general-purpose job, among the unit jobs, to the second processor preferentially over the first processor, the general-purpose job being a job executable for the first processor and the second processor (col. 5, lines 57-67, Abstract).

11. As to claim 13, it is rejected for the same reasons as stated in the rejection of claim 1.

12. As to claim 14, it is rejected for the same reasons as stated in the rejection of claim 1.

13. As to claim 15, it is rejected for the same reasons as stated in the rejection of claim 1.

14. As to claim 16, Dave teaches wherein: at least one of the unit jobs is executable for the first processor and the second processor in accordance with programs that are different from each other (have heterogeneous platforms/architecture) (col. 1, lines 35-45, Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dave et al. (hereinafter Dave) (US 6,112,023) in view of Cai et al. (hereinafter Cai) (US 2004/0003309 A1).

16. As to claim 4, Dave is silent in teaching a mode switching means for switching each processor between an operation mode and a power-saving mode, in accordance with a result of a process performed by the unit job scheduling means, the operation mode being a mode in which the processor is enabled to execute unit jobs, and the power-saving mode being a mode in which power consumption is lower than in the operation mode. However, Cai teaches an asymmetric processing system with a switching logic that switches execution from a regular operation mode to a reduced power consumption mode (Abstract, [0019], first two lines of [0020]). Dave and Cai are analogous art because they are both in the same field of endeavor of asymmetric processing and solving the same problem of power conservation. One of ordinary skill in the art would have known to modify Dave's asymmetric processing system such that it would include the feature of switching modes to a reduced power consumption mode, as taught in Cai. The suggestion/motivation for doing so would have been to provide the predicted result of improving the control of temperature and power consumption of electronic components such as processors

([0004]). Therefore, it would have been obvious to one of ordinary skill in the art to combine Dave and Cai to obtain the invention of Claim 4.

17. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dave et al. (hereinafter Dave) (US 6,112,023).

18. As to claim 5, Dave teaches having a first processor and a second processor that are heterogeneous (see Title, col. 1, lines 35-45). Dave is silent teaching that each processor has memory capacities that are different from each other. However, it is well known to one of ordinary skill in the art that heterogeneous processors that have different platforms/architectures, as taught in Dave, would require different memory capacities. Therefore, it would have been obvious to one ordinary skill in the art for Dave's heterogeneous processors to include memory capacities of each processor that are different from each other so that the appropriate size memory can be used for each specific type of processor needs.

19. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dave et al. (hereinafter Dave) (US 6,112,023) in view of Naylor (US 7,197,627 B1).

20. As to claim 6, Dave is silent in teaching wherein: the first processor is capable of executing an instruction set for executing unit jobs; and the second processor is capable of executing at least an instruction subset that is a part of the instruction set. However, Naylor

teaches a multiple processor arrangement having a first processor for processing a first set of instructions and a second processor for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions (see Abstract, col. 1, lines 40-51, col. 2, lines 25-28, etc.). Dave and Naylor are analogous art because they are both in multiprocessing arrangements and solving the same problem of conserving power. One of ordinary skill in the art would have known to modify Dave's multiprocessing system such that it would include the feature of having a first processor for processing a first set of instructions and a second processor for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, as taught in Naylor's multiprocessing system. The suggestion/motivation for doing so would have been to provide the predicted result of improving power conservation of the multiprocessor system (col. 1, lines 20-36). Therefore, it would have been obvious to one of ordinary skill in the art to combine Dave and Naylor to obtain the invention of claim 6.

21. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dave et al. (hereinafter Dave) (US 6,112,023) in view of Naylor (US 7,197,627 B1), and further in view of Kamano et al. (hereinafter Kamano) (US 2002/0010848 A1).

22. As to claim 12, Dave teaches a heterogeneous/asymmetric multiprocessing system that can execute heterogeneous/asymmetric jobs (that require different/heterogeneous execution times) as well as having general-purpose processors that can execute general-purpose jobs (Abstract, col. 1, lines 33-47, col. 5, lines 57-67). Dave is silent in teaching wherein: the first

processor is capable of executing an instruction set for executing unit jobs; and the second processor is capable of executing at least an instruction subset that is a part of the instruction set. However, Naylor teaches a multiple processor arrangement having a first processor for processing a first set of instructions and a second processor for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions (see Abstract, col. 1, lines 40-51, col. 2, lines 25-28, etc.). Dave and Naylor are analogous art because they are both in multiprocessing arrangements and solving the same problem of conserving power. One of ordinary skill in the art would have known to modify Dave's multiprocessing system such that it would include the feature of having a first processor for processing a first set of instructions and a second processor for processing a second set of instructions, the second set of instructions being a subset of the first set of instructions, as taught in Naylor's multiprocessing system. The suggestion/motivation for doing so would have been to provide the predicted result of improving power conservation of the multiprocessor system (col. 1, lines 20-36). Dave in view of Naylor is also silent in teaching an exclusive job for the first processor. However, Kamano teaches a data processing system that utilizes a general-purpose process/job for each processor and a special purpose process/job (exclusive job) for only a special purpose processor ([0008]). One of ordinary skill in the art would have known to modify Dave in view of Naylor's system such that it would include the feature of Kamano's multiprocessing system utilizing a general-purpose job and special purpose job, etc. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance, namely by lowering power consumption, lowering cost, as well as the size of the

processor ([0010]). Therefore, it would have been obvious to one of ordinary skill in the art to combine Dave, Naylor and Kamano to obtain the invention of claim 12.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Jaggar (US 5,568,646)** teaches a data processing system using multiple instruction sets. The second instruction set is a subset of the first instruction set. The nature of the second instruction set as a subset of the first instruction set enables the benefit of one-to-one mapping to be efficiently performed (see Abstract).
- **Tang (US 6,298,370 B1)** teaches an asymmetrical multiprocessor system that load balances the processor based on power and is capable of image processing and schedules execution based on priority (see Abstract, etc.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Kenneth Tang/
Examiner, Art Unit 2195